

AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in this application.

1. (Currently Amended) A computer system comprising:
a central processing unit (CPU) core for executing instructions;
a digital signal processing (DSP) core for processing data in accordance with ~~an~~
the instructions;
a data cache for storing temporary data associated with the DSP core;
a first buffer module for storing input data received by the DSP core;
a second buffer module for storing output data provided from the DSP core; and
an external memory for storing the temporary data, the input data, and the output
data,
wherein the input and output data are received by and provided from the DSP core
in series through the first and second buffer modules without going through the data
cache.

2. (Currently Amended) The computer system of claim 1, wherein the first
and second buffer modules each comprise:

an address ~~buffer~~ register for storing an address of the external memory;
an increment unit for increasing the address by one bit;
a buffer for storing either the input data or the output data; and
a multiplexer for addressing the buffer in response to lower bits of the address.

3. (Currently Amended) The computer system of claim 2, wherein the address of the external memory is ~~initialized~~ set by a ~~the central processing unit (CPU)~~ core.

4. (Original) The computer system of claim 2, wherein the buffer comprises a set of data registers.

5. (Original) The computer system of claim 2, wherein the buffer comprises valid bits that inform of current occupation state by data in the data registers.

6. (Original) The computer system of claim 1, wherein the external memory comprises a temporary data field, an input data field, and an output data field which are independently arranged therein.

7. (Currently Amended) The computer system of claim 2, wherein when the buffer is empty, a the CPU core carries out a pre-fill operation to serially read the input data from the external memory and stack the input data in the buffer.

8. (Currently Amended) The computer system of claim 2, wherein when the buffer is full, a the CPU core carries out a post-flush operation to store the output data of the buffer in the external memory.

9. (Currently Amended) The computer system of claim 2, wherein an auto-fill operation is carried out by the ~~buffer module~~ DSP core to stack the input data of the external memory in the buffer when the buffer is empty.

10. (Currently Amended) The computer system of claim 2, wherein if the buffer is full, the ~~buffer module~~ DSP core carries out an auto-flush operation to store the output data of the buffer in the external memory.

11. (Currently Amended) The computer system of claim 1, wherein the computer system is integrated on a chip, the chip comprising a the CPU core, the DSP core, the data cache, and the first and second buffer modules.

12. (Currently Amended) A method of accessing data in a computer system having a central processing unit (CPU) core, a digital signal processing (DSP) core, a data cache, a buffer, and an external memory, comprising the steps of:

accessing temporary data for the external memory through the data cache if data of the DSP core includes the temporary data;

executing a pre-fill operation to serially transfer input data to the buffer when the buffer is empty;

executing a post-flush operation to store output data of the buffer in the external memory when the buffer is full;

executing an auto-fill operation to stack the input data of the external memory in the buffer when the buffer is empty; and

executing an auto-flush operation to store the output data of the buffer in the external memory when the buffer is full,

wherein the input and output data are accessed in series without passing through the data cache.

13. (New) The computer system of claim 2, wherein the buffer of the first and second buffer modules is a sequential buffer.

14. (New) The method of accessing data in a computer system of claim 12, wherein the auto-fill and the auto-flush operations are performed by the DSP core and the pre-fill and the post-flush operations are performed by the CPU core.